AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor comprising:

transferring data from ~~a~~ the cache memory to ~~an aligner~~ a bypass path and a data path;

transferring the data to an aligner from the data path;

generating a sign bit for the data in the bypass path, wherein the generating comprises:

selecting a plurality of candidate bits from the data, and

generating the sign bit from the plurality of candidate bits dependent on a select signal, wherein the sign bit is generated independent of propagation of the data through the data path;

transferring the sign bit to the aligner ~~via a~~ from the bypass path;

arranging the data and the sign bit in the aligner into signed data; and

transferring the signed data to the another element~~,~~

~~wherein transferring data and transferring the sign bit occur in parallel~~.

2. (Currently Amended) The method of claim 1, further comprising:

adjusting the data during transfer to the aligner via ~~a~~the data path~~; and~~

~~selecting the sign bit during transfer to the aligner via the bypass~~.

3. (Cancelled)

4. (Previously Presented) The method of claim 3, further comprising:

processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU.

5. (Currently Amended) An apparatus for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor, comprising:

a data path connecting the cache memory to an aligner, wherein data is transferred from the cache memory to the aligner via the data path; and

a bypass path connecting the cache memory to the aligner, comprising:

a sign multiplexer for selecting a plurality of candidate bits from the data in the cache memory; and

a real-sign multiplexer for selecting a sign bit from the plurality of candidate bits dependent on a select signal, wherein the sign bit is selected independent of propagation of data through the data path,

~~wherein data is transferred from the cache memory to the aligner via the data path and~~

wherein the ~~a~~ sign bit ~~for the data~~ is transferred ~~from the cache memory~~ to the aligner ~~via~~ from the bypass path, and

wherein the aligner arranges the data and the signed bit into signed data and transfers the signed data to the another element.

6. (Currently Amended) The apparatus of claim 5, further comprising:

a select component for providing a select signal[[s]] to choose the sign bit ~~for the data~~ from a plurality of candidate bits.

7. (Cancelled)

8. (Original) The apparatus of claim 6, wherein the select component provides a signal to choose a part of the data and to generate the sign bit for the data based on an instruction from a CPU.

9. (Original) The apparatus of claim 5, wherein the aligner comprises a plurality of sub-aligners.

10. (Currently Amended) An apparatus comprising:

means for transferring data from a cache memory to a bypass path and a data path ~~an aligner~~;

means for generating a sign bit for the data in the bypass path, wherein the means for generating a sign bit for the data comprises:

means for selecting a plurality of candidate bits from the data, and

means for generating the sign bit from the plurality of candidate bits dependent on a select signal,

wherein the sign bit is generated independent of propagation of data through the data path;

means for transferring the sign bit to the aligner via ~~a~~ the bypass path;

means for adjusting the data during transfer to the aligner via the ~~a~~ data path;

means for adjusting the sign bit during transfer to the aligner via the bypass path;

~~means for selectively processing a part of data for use in generating the sign bit;~~ and

means for selectively processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU;

means for arranging the data and the sign bit into signed data; and

means for transferring the signed data to another element in a microprocessor

~~wherein the transfer of data via the data path and the transfer of the sign bit via the bypass occur in parallel~~.

11. (Currently Amended) An apparatus comprising:

a data path connecting a cache memory to an aligner;

wherein data is transferred from the cache memory to the aligner along the data path;

a bypass path connecting the cache memory to the aligner;

wherein the data is transferred from the cache memory to the bypass path, ~~aligner along the data path~~ and

wherein a sign bit ~~for the data~~ is transferred ~~from the cache memory~~ to the aligner ~~along~~ from the bypass path~~, and~~

~~wherein the transfer of data via the data path and the transfer of the sign bit via the bypass occur in parallel~~;

a select component in the bypass path for providing signals to select ~~choose~~ the sign bit for the data, wherein the select component comprises:

a sign multiplexer for selecting a plurality of candidate bits from the data; and

a real-sign multiplexer for selecting the sign bit from the plurality of candidate bits, ~~and~~

wherein the select component provides a signal for selecting ~~choosing~~ a part of the data to generate the sign bit for the data based on an instruction from a CPU; ~~and~~

wherein the aligner comprises a plurality of sub-aligners; and

wherein the aligner arranges the data and the sign bit into signed data .